Appendix I: AQA vs. ARMlite

ARMlite simulates a cut-down version of a 32-bit ARM processor. The AQA instruction set (as issued with each of the A-level exam questions to date) is also *based on* the ARM instruction set, though cut down even further, and not followed as rigorously. AQA does not specify the word size, and specific exam questions have sometimes suggested that a register is 16, or even 8 bits wide. In practice, this lack of definition is not a big issue, since exam questions tend to deal with small data values - in which case it would make no difference if a register was 8,16 or 32 bits wide.

The AQA instruction set is limited to these instructions:

`LDR`, `STR`, `ADD`, `SUB`, `MOV`, `CMP`, `B`, `BEQ`, `BNE`, `BGT`, `BLT`, `AND`, `ORR`, `EOR`, `MVN`, `LSL`, `LDR`, and `HALT`

Chapters 1 – 4 of this book use only those instructions, and in a manner consistent with the AQA instruction set, which, to date, is included with each exam question on assembly language. Students should be aware that in an exam, they may use only those instructions and only in the ways spelled out on the instruction sheet included in the exam.

AQA specifies that `LDR` and `STR` take, as their second operand, a `<memory ref>`. Surprisingly, AQA does not specify exactly what form(s) this `<memory ref>` may take. However, as of the time of writing this book, the following may be *inferred* from past questions:

- `<memory ref>` is a *direct* address. AQA has never, to date, made any use of, or reference to, indexed or indirect addressing modes. The AQA exam questions to date have involved simple programming exercises where there is no need for indexed/indirect addressing, and where the latter would confer no advantage. Nonetheless, students that have learned these approaches should be clear that they should not use indexed/indirect modes in an exam.
- `<memory ref>` is a *decimal* number. AQA has not, to date, specified any direct *address* in hexadecimal or binary. Nor has AQA, to date, made use of a *label* as a memory address (labels have been used, to date, only to label instructions – not memory addresses).
- Although AQA has not, to date, specified it, we may infer from past questions, that `<memory ref>` is a 'word address'. ARMlite, in common with the ARM and most other modern processors, uses 'byte addressing'.

The last point is the most important one to understand. Assuming AQA does mean *word addressing* (and assuming *decimal* addresses), then the following AQA code:

```
LDR R0, 100
LDR R1, 101
```

would result in registers `R0` and `R1` being loaded with two different values from two successive words in memory. With ARMlite, and on a real ARM processor, the second instruction would give an assembly error ('`Unaligned address …`') because the second address would be only 1 *byte* after the first, and legitimate word addresses must be divisible by 4.